

CHT-RIGEL- DATASHEET

Version: 1.6
20-Dec-23
(Last Modification Date)

High-Temperature, Adjustable, Linear Voltage Regulator +0.9V to +28V / 100mA

General description

The CHT-RIGEL is a high-temperature, high-reliability, 100mA adjustable linear voltage regulator suitable to generate from a +4.5V to +30V voltage source any regulated voltage in the range +0.9V to +28V. Its operating junction temperature ranges from -55°C to +225°C and can possibly go outside that range with some de-rating of the performance. The regulator is self-protected with a built-in current limiter and a thermal protection, the later becoming effective in the range 250°C to 300°C. CHT-RIGEL brings unique benefits in applications where the ambient or operating temperature is high and above the temperature supported by traditional semiconductors, or in applications that run in standard 125°C or 150°C, possibly 175°C but require extended reliability: CHT-RIGEL brings at least an order of magnitude in lifetime compared to traditional silicon solutions. It allows as well accelerated aging of the systems for qualification purposes as the device can support extreme temperatures.

The IC features a chip-enable (CE active low) input signal allowing placing the circuit in low-power, disable mode.

The output voltage is adjustable by the external resistive feedback.

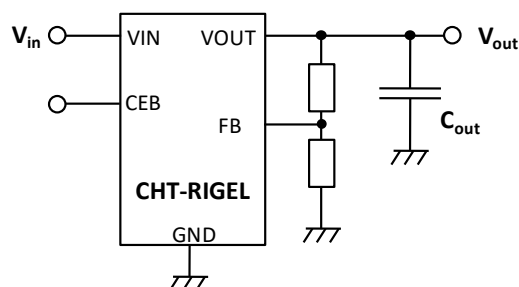
The CHT-RIGEL is a one-die solution, available in a tiny ceramic package TDFP-16 for applications where small PCB footprint is critical.

Applications

- Regulated power supplies for embedded electronics in down-hole, aerospace and industrial systems.

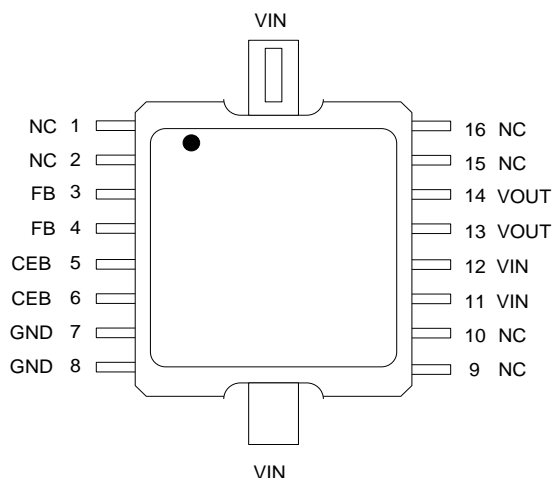
Features

- Junction operating temperature from -55°C to 225°C
- Input voltage from 4.5V to 30V
- Output voltage: from 0.9V to 28V
- Output voltage total accuracy: $\pm 5\%$ ¹
- Output current: 100mA max
- Min voltage dropout @ 100mA: 1.7V
- Line regulation: -1% max
- Load regulation: -0.2% max
- C_{out}: min 1 μ F (2.2 μ F for V_{out} below 1.8V)
- Chip Enable (active low)
- Input ripple rejection: 65dB typ (@ 100Hz)
- Quiescent current (no load, Chip Enable active, 225°C): 1.1 mA typ.
- Stand-by current (no load, Chip Enable inactive, 225°C): 40 μ A typ.
- Thermal shutdown: Active in the range 250°C to 300°C
- Current limitation: 200 mA typ.
- Latch-up free
- Available in TDFP16
- Validated at 225°C for 1000 hours (and still on-going)



¹ Excluding accuracy of external components but including initial accuracy variation, temperature variation, line and load regulation variations

Pinout



Pin #	Pin Name	Pin Description
1	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
2	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
3	FB	Input pin; feedback pin to be connected via a resistor network to Vout (cfr Typical application diagram on page 1)
4	FB	Input pin; feedback pin to be connected via a resistor network to Vout (cfr Typical application diagram on page 1)
5	CEB	Input pin; Chip Enable pin; when connected to GND, CHT-RIGEL is active; with voltage on CEB higher than $V_{IH\ CEB}$, VOUT is tied to GND and CHT-RIGEL enters in a low-power mode
6	CEB	Input pin; Chip Enable pin; when connected to GND, CHT-RIGEL is active; with voltage on CEB higher than $V_{IH\ CEB}$, VOUT is tied to GND and CHT-RIGEL enters in a low-power mode
7	GND	Negative power supply
8	GND	Negative power supply
9	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
10	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
11	VIN	Positive power supply
12	VIN	Positive power supply
13	VOUT	Output voltage
14	VOUT	Output voltage
15	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
16	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing

The 2 vertical large leads are internally connected to VIN and are also connected to the package heat sink.

Absolute Maximum Ratings

Supply Voltage Vin to GND	-0.5 to 35V
Voltage on CEB and FB	max Vin
Peak output current	Internally limited
Junction Temperature (Tj)	250°C

Operating Conditions

Supply Voltage Vin to GND:	4.5V to 30V
Junction temperature	-55°C to +225°C
Continuous current	0 to 100 mA

ESD Rating

Human Body Model	>4kV
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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability. Permanent uses of the device in short-circuit state or in over-temperature state may affect long term reliability of the device.

Electrical Characteristics

Unless otherwise stated, $T_j = 25^\circ\text{C}$, $C_{in} = 4.7\mu\text{F}$, $C_{out} = 4.7\mu\text{F}$. **Bold** figures point out values valid over the whole temperature range ($T_j = -55^\circ\text{C}$ to $+225^\circ\text{C}$).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	V_{in}		4.5		30	V
Output voltage range	V_{out}	$V_{in} = [4.5\text{V}-25.9\text{V}]$	0.9		Vin-1.7V	V
		$V_{in} = [25.9\text{V}, 30\text{V}]$	Vin-25V		Vin-1.7V	V
Dropout ¹	D_r	$I_{out} = 100\text{mA}$	1.7		25	V
Output current	I_{out}		0		100	mA
Output voltage total accuracy		$V_{in} = [4.5-30]\text{V}$ $I_{out} = [0 \dots 100]\text{mA}$	Vout -5%		Vout +5%	V
Output voltage temperature drift		$V_{in} = 5\text{V}$; $V_{out} = 1.8\text{V}$ $I_{out} = 0\text{mA}$ $T_j = [25^\circ\text{C} - 225^\circ\text{C}]$		+2.2		%
Output voltage line regulation		$V_{in} = [4.5-30]\text{V}$; $V_{out} = 1.8\text{V}$ $I_{out} = 0\text{mA}$			-1	%
Output voltage load regulation		$V_{in} = 5\text{V}$; $V_{out} = 1.8\text{V}$ $I_{out} = [0 \dots 100]\text{mA}$		-0.06 ²		%
		$V_{in} = 30\text{V}$; $V_{out} = 27\text{V}$ $I_{out} = [0 \dots 100]\text{mA}$		-0.183		%
Quiescent current ³	I_q	$V_{in} = 5\text{V}$; $V_{out} = 1.8\text{V}$ $I_{out} = 0\text{mA}$		1		mA
		$V_{in} = 30\text{V}$; $V_{out} = 1.8\text{V}$ $I_{out} = 0\text{mA}$		1.15		mA
Standby current ⁴	I_{stdby}	$V_{in} = 5\text{V}$; $T_j = 225^\circ\text{C}$ $CEB = 5\text{V}$		7		μA
		$V_{in} = 30\text{V}$; $T_j = 225^\circ\text{C}$ $CEB = 5\text{V}$		40		μA
Response to Line Transient		V_{in} from 5V to 10V (5V/ μs) $V_{out} = 1.8\text{V}$; $I_{out} = 50\text{mA}$		+5		%
		V_{in} from 10V to 5V (5V/ μs) $V_{out} = 1.8\text{V}$; $I_{out} = 50\text{mA}$		-5		%
		V_{in} from 5V to 6V (5V/ μs) $V_{out} = 1.8\text{V}$; $I_{out} = 50\text{mA}$		+1		%
		V_{in} from 6V to 5V (5V/ μs) $V_{out} = 1.8\text{V}$; $I_{out} = 50\text{mA}$		-1		%
Response to Load Transient		$V_{in} = 10\text{V}$; $V_{out} = 2.5\text{V}$ I_{out} from 10mA to 100 mA (10mA/ μs), $T_j = 225^\circ\text{C}$		-5		%
		$V_{in} = 10\text{V}$; $V_{out} = 2.5\text{V}$ I_{out} from 100 mA to 10 mA (10mA/ μs), $T_j = 225^\circ\text{C}$		+7		%
Power Supply Rejection Ratio ($V_{in} = 10\text{V}$, $V_{out} = 1.8\text{V}$, $I_{out} = 10\text{mA}$)	PSRR	100Hz		65		dB
		1 KHz		45		dB
Output noise voltage		$BW = [1\text{Hz} \dots 10\text{KHz}]$ $V_{out} = 1.8\text{V}$; $T_j = 25^\circ\text{C}$		37		μV_{RMS}
Short-circuit current	I_{SC}	$V_{in} = [4.5-30]\text{V}$	110	200	260	mA
FB input current	I_{FB}	$V_{in} = 10\text{V}$; $T_j = 225^\circ\text{C}$ $V_{FB} = 0.9\text{V} \pm 10\%$		50		nA
CEB input current	I_{CEB}	$V_{in} = 5\text{V}$; $V_{CEB} = 5\text{V}$; $T_j = 225^\circ\text{C}$		3		μA
CEB V_{IL}	$V_{IL\ CEB}$				1.2	V
CEB V_{IH}	$V_{IH\ CEB}$		2			V
Over temperature protection threshold	TH_{OTP}			285		$^\circ\text{C}$
Over temperature protection hysteresis	$Hyst_{OTP}$			10		$^\circ\text{C}$
Junction-to-case thermal resistance	$R_{\theta JC}$			11		$^\circ\text{C/W}$

¹ Refer to Figure 16 for evolution of min dropout in function of required output current

² Load regulation measurements must be done in a way to avoid self-heating effect

³ Current through feedback resistances excluded

Typical Performance Characteristics

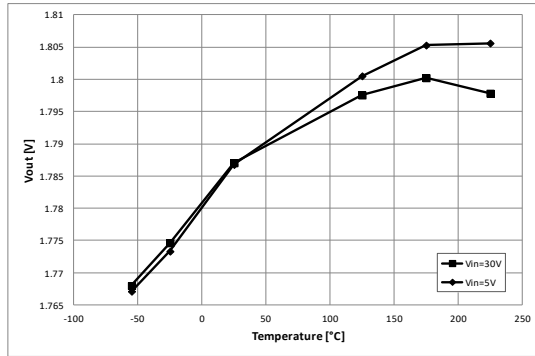


Figure 1: Output voltage temperature drift ($I_{out} = 0 \text{ mA}$)

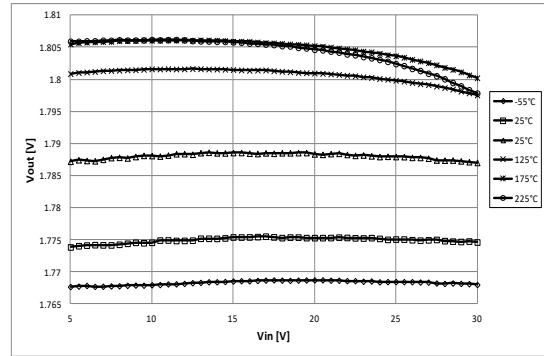


Figure 2: Output voltage line regulation ($I_{out} = 0 \text{ mA}$)

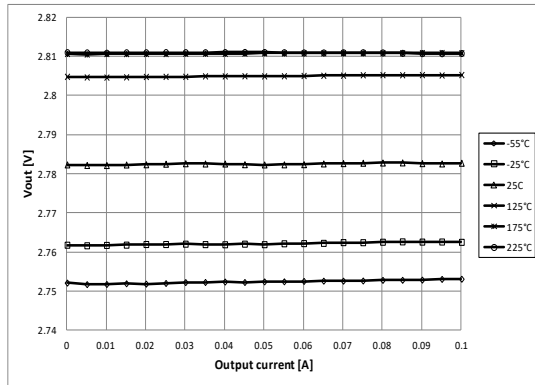


Figure 3: Output voltage load regulation ($V_{in} = 4.5 \text{ V}$, $V_{out} = 2.8 \text{ V}$)

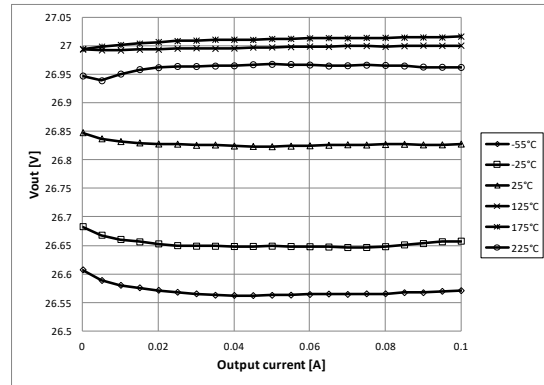


Figure 4: Output voltage load regulation ($V_{in} = 30 \text{ V}$, $V_{out} = 27 \text{ V}$)

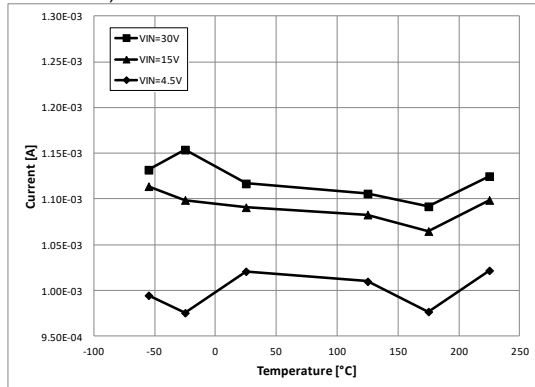


Figure 5: I_q versus temp ($V_{out} = 1.8 \text{ V}$, $I_{out} = 0 \text{ mA}$)

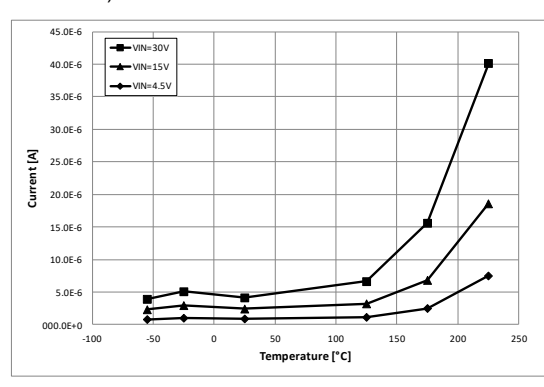


Figure 6: I_{stdby} versus temp

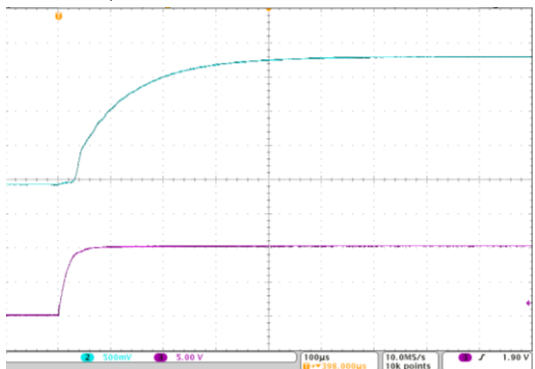


Figure 7: Start-up transient
($V_{in} = 0$ to 10 V , $1 \text{ V}/4 \mu\text{S}$; $V_{out} = 1.8 \text{ V}$, $I_{out} = 10 \text{ mA}$, $T_a = 225^\circ\text{C}$)(2:Vout,3:Vin)

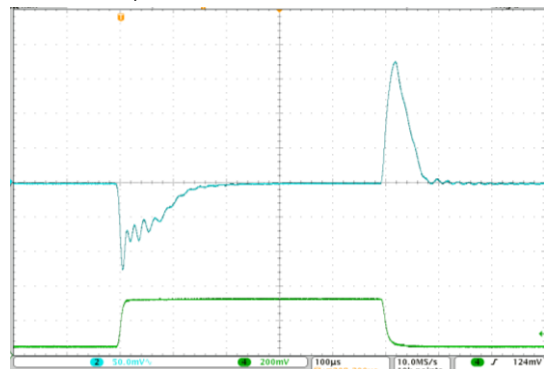


Figure 8: Response to load transient (10mA to 100 mA, 100 mA to 10mA, 10mA/ μs , $V_{in} = 10 \text{ V}$, $V_{out} = 2.5 \text{ V}$, $T_a = 225^\circ\text{C}$, $C_{out} = 4.7 \mu\text{F}$) (2:Vout AC, 4:Iout)

Typical Performance Characteristics (cnt'd)

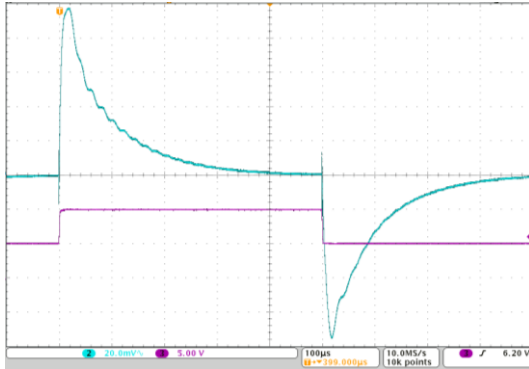


Figure 9: Response to line transient ($I_{out} = 50 \text{ mA}$, V_{in} : 5 to 10V, 10V to 5V; $5 \text{ V}/\mu\text{s}$, $V_{out} = 1.8 \text{ V}$, $T_a = 225^\circ\text{C}$; $C_{out} = 4.7\mu\text{F}$) (3: V_{in} , 2: V_{out} AC)

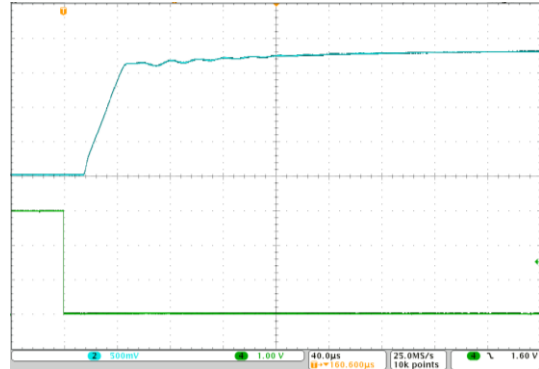


Figure 10: Transition from disabled state ($V_{in} = 10 \text{ V}$, $V_{out} = 1.8 \text{ V}$, $C_{out} = 4.7\mu\text{F}$, $I_{out} = 10 \text{ mA}$, $T_a = 225^\circ\text{C}$) (4: CEB, 2: V_{out})

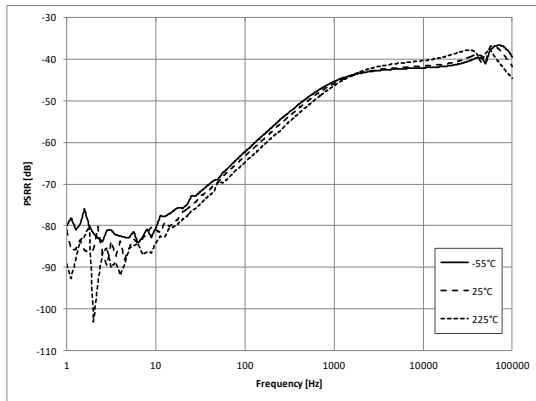


Figure 11: PSRR ($V_{in} = 10 \text{ V}$, $V_{out} = 1.8 \text{ V}$, $C_{out} = 4.7\mu\text{F}$, $I_{out} = 10 \text{ mA}$)

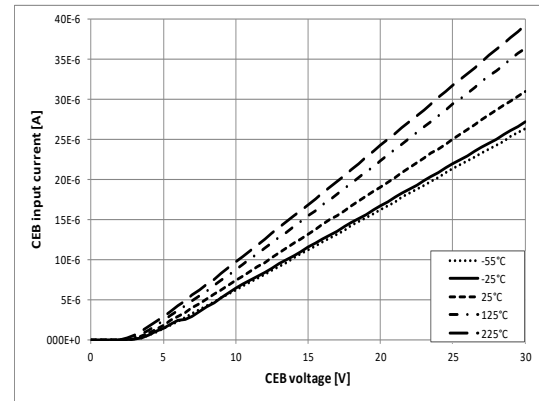


Figure 12: CEB pin input impedance

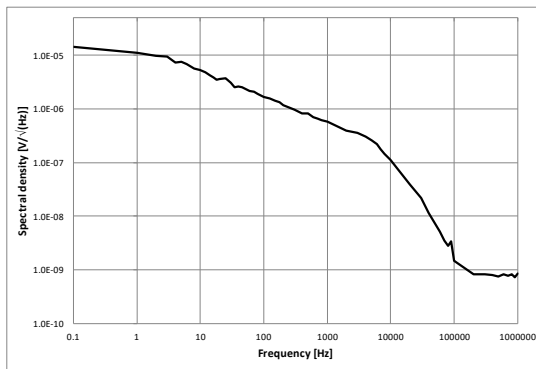


Figure 13: Output noise spectral density ($V_{in} = 8 \text{ V}$, $V_{out} = 1.8 \text{ V}$, $I_{out} = 0 \text{ mA}$, $C_{out} = 4.7 \mu\text{F}$, $T_a = 25^\circ\text{C}$)

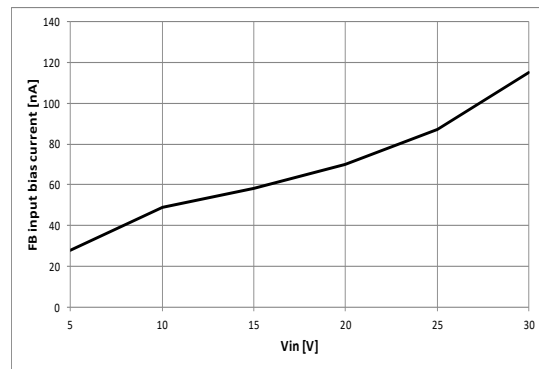


Figure 14: FB pin input leakage current (225°C)

Circuit Functionality

Safe operating area, power dissipation, and PCB layout considerations:

The tiny TDFP package used for CHT-RIGEL requires adequate PCB layout in order to achieve efficient thermal dissipation, the minimization of the junction operating temperature, and maximizing the power dissipation taking advantage of the temperature behavior capability of CHT-RIGEL.

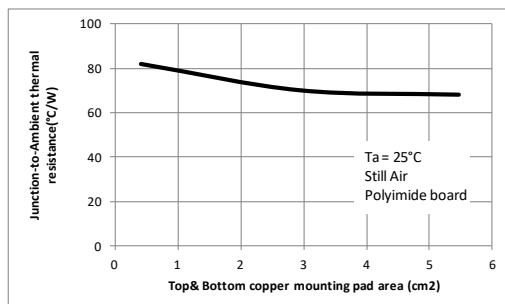
The junction-to-air overall thermal resistance of CHT-RIGEL in TDFP package relies, to a large extent, on the implementation of the copper mounting pads that act as a heatsink for the integrated circuit. The design must take into consideration the size of the copper pad and its placement on either of the board surfaces, or both.

The maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and junction-to-ambient thermal resistance:

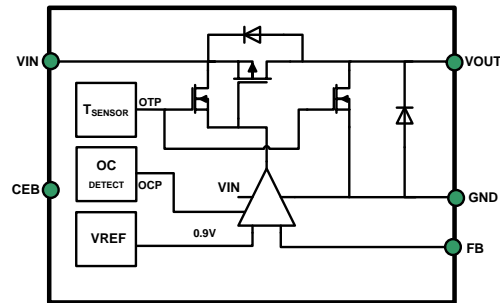
$$P_{DMAX} = (T_{JMAX} - T_A) / R_{\theta JA}$$

Where $T_{JMAX} = 225^{\circ}\text{C}$ and $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$ with $R_{\theta JC} = 11^{\circ}\text{C/W}$ and $R_{\theta CA}$ (to be determined) is function of the size of the copper mounting pad and thermal coupling to the TDFP16.

The graph below indicates the junction-to-air thermal resistance of the TDFP package mounted on PCB versus the surface of the copper thermal pads on the PCB. The designer should refer to this graph when designing his PCB layout, taking into account his own operating configuration: expected power dissipation (calculated from maximum input voltage, the output voltage and the expected current flow thru CHT-RIGEL) and the maximum expected ambient operating temperature.



Functional Block diagram



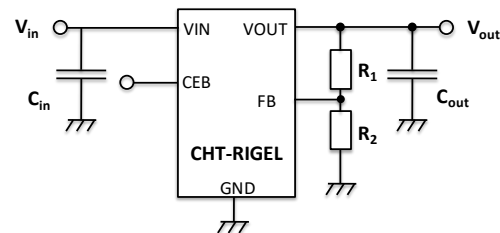
A PMOS transistor controls the level of current flowing from VIN to VOUT. An internal voltage reference of 0.9V (highly stable over the whole temperature range) provides the reference to which the voltage on the FB pin is compared. The internal amplifier drives the gate of the PMOS and regulates VOUT.

An on-chip temperature sensor with hysteresis monitors the die temperature; if this die temperature exceeds a predefined threshold, the PMOS transistor is disabled and VOUT is connected to GND.

In addition, an overcurrent protection circuit is implemented which limits gracefully the output current to a pre-defined value.

A Chip Enable function is provided thru the CEB pin: when tied low, the CHT-RIGEL is enabled and operates normally; when CEB is tied high, CHT-RIGEL is disabled. Note that the disable circuitry acts in the same way as the over-temperature disabling scheme as described above.

External resistances calculation rules



R1 and R2 values should be computed as follows:

$$\frac{R1 + R2}{R2} = \frac{VOUT}{0.9V}$$

R1+R2 value should be lower than 200kΩ to limit the impact of the FB input leakage

current. For $V_{out} = 0.9V$, V_{out} signal can be tied directly to FB pin

Input and output capacitance

CHT-RIGEL requires an output capacitor connected between V_{OUT} and GND to stabilize the internal control loop. The output capacitance value must be between $1 \mu F$ and $10 \mu F$ for V_{out} higher or equal to $1.8V$ and between $2.2 \mu F$ and $10 \mu F$ for V_{out} below $1.8V$; in both cases, ESR (equivalent series resistance) value should be between 0.01Ω and 1Ω .

Higher capacitor values offer improved behaviour in case of fast and high amplitude load transient.

There is no explicit requirement on the value of the input capacitance. Its size mainly depends on system aspects (impedance of the power source, distance between power source and CHT-RIGEL, amount and speed of the load transients ...). CISSOID recommends the use of a $1 \mu F$ input capacitance.

CEB input

CEB input pin internal circuit is depicted in Figure 15.

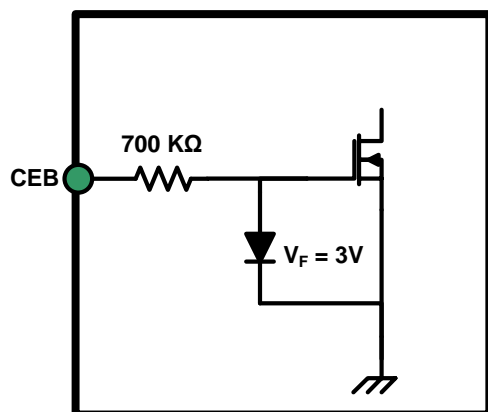


Figure 15

CEB threshold is set by the threshold of the transistor T1 (value between 1.2 and $2V$).

It is expected that CEB pin will be driven by a controller and so that the CEB control signal voltage range will be typically between $0V$ and $[3.3V-5V]$; in this case, the leakage current through the CEB pin will be $3 \mu A$ typ. over the whole temperature range.

Would the application use a larger voltage swing to control the CEB pin, system designers should take into account that CEB pin will present an additional equivalent resistance of about $700K\Omega$.

Current limit

In case the load connected to CHT-RIGEL would demand more than $100 mA$ current, the internal current limiter circuit will limit the maximum current delivered by CHT-RIGEL to $200mA$ (typical) whatever the output voltage.

If the output current exceeds the recommended $100mA$ and depending on the conditions (dropout, junction-2-air thermal resistance), the internal thermal protection could get activated and CHT-RIGEL would then switch between 2 modes:

- Thermal protection active; no output current
- Thermal protection not active; output current internally limited.

In case of short-circuit, both current limiter and thermal protection will be activated and will protect the device. Endurance tests have been performed and showed that CHT-RIGEL did resist to a permanent short-circuit ($V_{in} = 30V$) for at least 8 hours.

Dropout

Dropout at $100mA$ output current is specified to be $1.7V$ minimum.

If the application requires less current, minimum required dropout value decreases. Figure 16 provides guidance on the evolution of the minimum dropout with the output current.

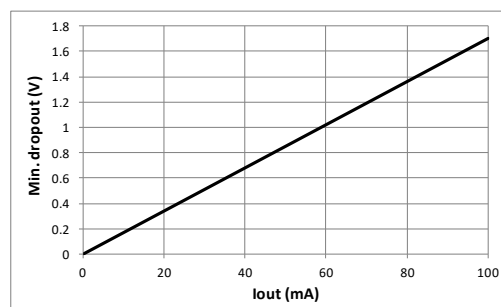
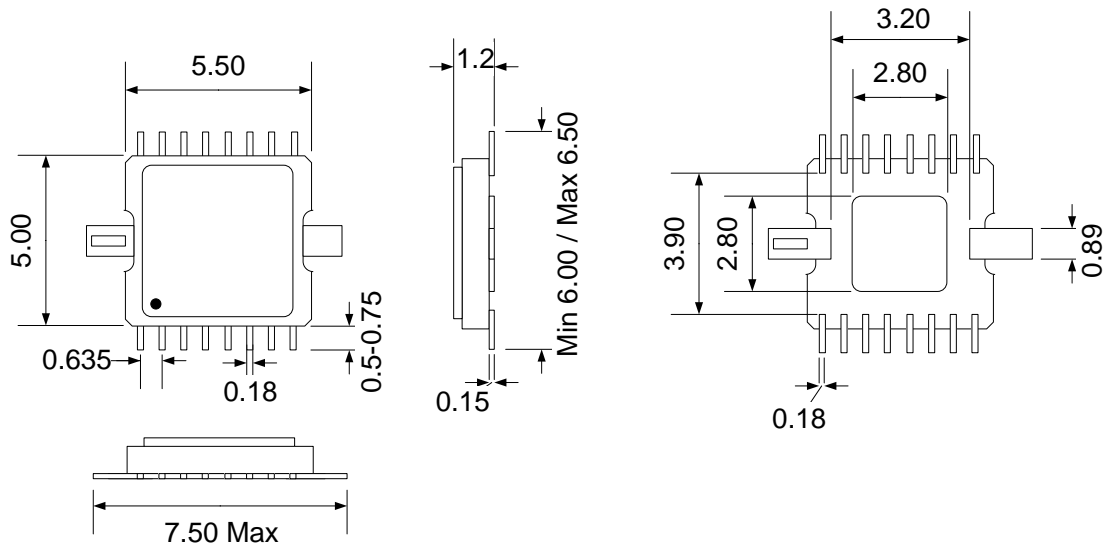


Figure 16

Package Dimensions



TDFP16 physical dimensions (mm +/-10%)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CHT-RIGEL	CHT-STA5602C-TDFP16-T	TDFP16	CHT-STA5602C

Contact & Ordering

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